

## **A Report on EPTC 2008**

Electronics Packaging Technology Conference  
9<sup>th</sup> to 12<sup>th</sup> December 2008  
Grand Copthorne Waterfront Hotel, Singapore

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The 10<sup>th</sup> Electronics Packaging Technology Conference (EPTC 2008) took place from the 9<sup>th</sup> to the 12<sup>th</sup> December 2008 at the Grand Copthorne Waterfront Hotel, Singapore. The three day conference had been organised by the IEEE Reliability/CPMT/ED Singapore chapter and was preceded by a day of seven short courses and a VIP dinner cruise on the South China Sea. There was also an exhibition that was attended by companies and organisations supporting the event. The first day of the conference was dedicated to a number of keynote presentations and a plenary session, while on the following two days the conference was divided into six parallel sessions covering a wide range of subject material.

Following a short opening ceremony, which included traditional drum music and two 'dancing lions' taking to the stage, there was a review of the evolution of the EPTC conferences, from the first one held in 1997 to the current event. This 10<sup>th</sup> Anniversary Conference had over 400 attendees and almost 50 technical sessions. The opening welcome was given by William Chen, President of the IEEE/CPMT Society, who thanked the organisers for all their hard work in organising the event. Dr Alastair Trigg then added his congratulations to EPTC and noted that this was the biggest conference yet.

The first keynote presentation was given by Professor G. Q. Zhang of NXP and Delft University of Technology in Holland and was entitled 'The Changing Landscape of Semiconductor Industry - more than just ICs'. He began by stating that, although the industry was currently in difficult times, there was light at the end of the tunnel and packaging was the key to the future. Professor Zhang then reviewed progress over the last 30 years in various areas of electronics and he suggested that, for the future, society needed ambient intelligence that was embedded, context aware, personalised and adaptive. He then described that, in total, electronics was currently valued at \$1340 billion. Trends and Moore's Law were then discussed. There were currently devices with over 1.6 billion transistors incorporated on a single silicon chip and transistors currently cost around 1 millionth of what they cost in 1968. For the future, there were a number of different ways forward, both in terms of improving traditional devices and with new types. However, packaging and assembly technology would also have to be improved.

The move to 'More than Moore' was also described and an example of an intelligent system was discussed, namely sensing, which integrated additional non-digital capabilities. This would need an approach described as hetero-integration packaging. Professor Zhang also raised the issue of what would be the role of less advanced wafer fabs in the future in the context of sustainability and employment etc. He then discussed business trends and industry observations. In some years there had been large growth but there were also years with high negative growth. Since 2000 there had been slower market growth which approximately correlated with GDP. Cash was the key in the credit crunch and fewer companies now had the funds to build new wafer fabs or even to support the R&D costs. Challenges for the future were about much more than miniaturisation; there was, for example, a gap between design and technology and there was a need to solve the hardware and software design gap. There was also a growing diversification in the types of materials used and this required the use of many more elements from the periodic table. Another concern for the future was the fact that there were also many new failure types emerging, some of which were highly complex and interrelated. For the future, there was a need to develop 'Moore alike' eco-systems and the supply chain for 'More than Moore'. Professor Zhang concluded that there was a bright future for electronics and he detailed what he described as the 'innovation and business waves'. The third wave, which began in 2005, was about 'More than Moore' and a key additional challenge for the future would be around 'master system creation'.

The second keynote speech was given by Professor Michael Pecht, Director of CALCE at the University of Maryland, and was entitled 'A New Approach to Qualification Testing'. He began by saying that products were changing rapidly, supply chains were becoming more complex and yet reliability issues were becoming increasingly important. Some notable examples of recent reliability issues were highlighted. Companies conducted significant levels of qualification testing using accelerated test regimes such as HAST and they normally assumed that the results could be related to typical in-use reliability and end-user conditions. However, there was a growing and widening range of conditions under which devices were typically used today and these needed to be taken into account during qualification. Michael also advised that

it was important to beware of 'typical standards', as they might not cover real-life operating conditions. Examples of the temperature and shock profiles of an aircraft and a computer monitor were shown which demonstrated the unexpected extreme conditions that they had experienced. Other challenges in qualification included the fact that failures were sometimes intermittent and that there was often not enough time to test to failure. There was thus a move to prognostics based qualification methodologies because these could reduce the qualification times of products. This included a number of approaches such as probabilistic physics of failure models and data driven prognostics-based qualification analysis. Examples relating to the reliability of multilayer ceramic capacitors and computers were then discussed. In the case of the computer, 54 different parameters were monitored and the approach compared data from the test system with that of a healthy system used for correlation. In future, fusion based prognostics would become increasingly important and prognostics would be incorporated into all electronics.. Overall, the aim was to provide an early warning of failures, to provide guidance to extend useful life and to forecast maintenance as needed.

The final key note presentation of the morning was given by Professor C. P. Wong from Georgia Tech and was on the subject of 'recent advances on polymers and polymeric nano-composites for advanced electronics packaging applications'. He began by discussing why nano-materials were of interest for electronic packaging. The reasons included their potentially superior electrical, chemical, mechanical and optical properties. The example of quantum dots for bio-labelling and bio-imaging and the work being carried out at U. C. Berkeley was then presented. The six main parameters of electronic packaging were introduced and the evolution of electrically conductive adhesives (ECAs) as replacements for conventional solders was discussed. Work had been carried out to enhance the current carrying capability of ECAs via the use of self-assembling monolayers (SAMs), which selectively bonded to certain metals. The use of high K nano-composites to make novel capacitors was also described. Dielectric constants of up to 13,000 had been achieved, although there were some issues with loss values. An alternative approach used a barium titanate-epoxy composite cured with a suitable metal chelating agent. Work on lead-free solders was also discussed and it had been found that, with nano-particles, the melting points could be reduced by as much as 40 degrees, although they also became increasingly reactive and thus needed protection from oxidation using a surfactant capping agent. Professor Wong then introduced the newer forms of carbon such as C<sub>60</sub>, graphene and carbon nano-tubes (CNTs) and described their unique properties. CNTs showed promise in thermal management applications and methods of making these materials were given. For electronic applications, CVD methods were particularly attractive, as the materials could be grown in large area arrays on silicon wafers. Applications in flip chip

and wafer level packaging were also discussed. Professor Wong concluded his presentation with a discussion of the potential for nano-materials in self-cleaning applications using a nano-texturing approach with gold assisted etching.

The afternoon of the 10<sup>th</sup> December was then dedicated to a plenary session with presentations from a number of distinguished invited speakers. The first of these was by William Chen, President of the CPMT Society and it was on the subject of 'Rethink Engineering in the Era of Consumer Electronic Market'. He began by stating that consumer electronics was dominating the market and the global economy meltdown was impacting both consumer and corporate spending. Already, over 50% of the semiconductor market was dedicated to consumer electronics and this percentage would continue to increase. The global electronics market was currently valued at \$1.3 trillion, a figure larger than the GDP of India. There had been a proliferation of potential packaging solutions and 3D packaging offered a number of benefits, particularly where there was a need to package heterogeneous device assemblies. Dr Chen concluded that there was a need to rethink the engineering role in the very interesting times faced by the electronics industry.

The next paper was from Hirofumi Nakajima of NEC, Japan and his talk was on 3D system integration and where it was going. He began by stating that it was heading for the market and that the required R&D was being guided by the demand roadmaps from organisations such as ITRS and JISSO. The demand in the home electronics market was discussed and the example of demand for 10 mega-pixel image sensors in digital stills cameras was provided as an example. In the cellular phone market, SiP and SoC packages were being used because of the demand for increased functionality. The automotive electronics sector required integrated devices of sensors, electronic components and semiconductors and flip chip BGA was one example of the package types increasingly used. A key challenge was for high speed access to large capacity memory modules and this could be achieved using stacked die. The evolution of developing technologies by various Japanese companies was discussed. A concept called 'Dream Chip' was described and this had the target of developing multi-functional 3D integration as a core technology to build a flexible, reconfigurable 3D IC with new functions. The JISSO 2007 Roadmap's packaging development requirements out to 2020 were shown and the various activities around the world to meet these requirements highlighted. It was increasingly likely that future developments would best be handled by consortia rather than individual companies.

The next presentation was from John Lau of IME and he spoke about 'enabling technologies for 3D IC integration and packaging'. Devices were increasing both in size and I/O levels and there was an increasing need for new packaging technologies. These included through silicon vias (TSVs), improved thermal

management, solder bump technology and low-temperature bonding. There was also a need for thin wafer handling technology. In the case of TSVs, these could be produced by deep ion etching or by using a laser. These vias were typically filled with copper but this took a long time and the process had low throughputs. John then discussed the effects of TSV interposers on the reliability of large die. The copper filled vias could actually help to enhance the thermal performance but also increased the thermal expansion coefficient. Liquid cooling solutions for 3D stacked modules were also shown and there was a DARPA project to develop this approach. Low temperature bonding was then described; this was a process that used a very low melting point solder to achieve 3D stacking and which formed a high temperature remelting alloy. The application of stress sensors in wafer thinning applications was also described.

Professor Herbert Reichl of the Fraunhofer IZM in Berlin, Germany then discussed the European perspective on 3D integration. Key application areas included transport and mobility, energy and environment, health and car, security and safety and communications and consumer electronics. 3D system integration offered a wide range of benefits including increased reliability and reduced size. Advanced technologies included embedding ultra thin chips in flex substrates and also in conventional PCBs. An example of the Fraunhofer's 3D thin chip approach was shown that had three chips and a BCB/Cu redistribution layer. In the case of TSVs, there was currently no standard technology and there were questions about guaranteeing the reliability. Typical TSV aspect ratios were between 3:1 and 10:1. The European funded 'e-Cubes' project was also mentioned and it was stated that the EU was providing financial support for such collaborative projects.

Professor Rao Tummala from Georgia Institute of Technology then gave a presentation on the US perspective on 3D integration in a presentation called 'Beyond 3D ICs with TSVs'. The two main applications of TSVs were in 3D ICs with TSVs and 3D systems with TSVs. The 3D systems with TSVs could compensate for IC performance beyond the 32 nm node and they offered a low-cost approach to an entire system. Examples of 3D ICs and 3D systems were shown and the 3D system incorporated a wide range of different types of devices and interconnections made of silicon, metals and alloys, ceramics, organics and composites at the micron to millimetre range.

The final presentation of the session was from Professor Keyun Bi, Vice President of the China Semiconductor Packaging Association in China. In 2007, China produced 41.16 billion ICs, a 22.6% increase on the previous year and it was stated that China had 280 organisations doing work on electronics packaging; the key ones being Freescale Semiconductor and Qimonda. Much Chinese production was on low-end applications but the demand for more complex, high density, high pin count

and fine pin packaging such as MCM, WLCSP, CSP and MEMS, was increasing.

The afternoon plenary session concluded with a panel discussion and there was also a publication workshop which was chaired by Ricky Lee. In the evening the delegates were treated to a gala banquet at the Singapore Turf Club, where they had a chance to watch a number of horse races and to network with other delegates.

During the second and third days, the conference divided into multiple parallel sessions. The following text therefore gives a brief review of some representative examples of papers from the sessions attended by the writer. For further information, and more details of all the papers, reference should be made to the conference proceedings<sup>1</sup>.

The first speaker in the 'Advanced Interconnects 1' session was given by Dr Yong Liu of Fairchild Semiconductor, Portland, USA. This invited paper was entitled 'Trends in Power Packaging and Modelling'. He began by describing the power conversion market and stated that 51% of energy consumption was associated with motion. The challenges of power packaging and modelling were then outlined and these included die shrinkage, reduced wire bond pitch, higher current density and associated issues such as heat dissipation and electromigration. Also, there were demands for new materials for power chips such as silicon carbide and gallium nitride i.e. wide band gap materials with high breakdown voltages, low on-resistances and high thermal conductivities. Existing modelling tools needed development to accommodate electromigration and package bump systems. Trends in discrete power MOSFET packages were shown; the use of epoxy moulding compounds was decreasing as a percentage of the total package count, however, they were still useful for discrete devices. With the demand for smaller package footprints, integration of the heatsink into the package was becoming an increasingly important requirement. Examples of side by side placed multiple die and stacked die power SiP devices were then shown.

The second paper on 'Glass as a Substrate for High Density Electrical Interconnects' was given by Dr David Hutt of Loughborough University. David began by confirming that high density substrate manufacture was needed to match the fine features of silicon devices. Glass was a potential alternative substrate to the more conventional organic substrates and it could offer good dimensional stability, as well as high temperature and good insulation properties. Work had been undertaken towards building a multilayer substrate using CMZ glass sheets. Techniques used in this work included laser machining of glass with a KrF excimer laser to produce microvias and tracks. Methods had been developed to optimise the shapes of the microvias and one approach had been to apply a protective sacrificial film on the surface during drilling. Microvias with an entry diameter of 100 µm and exit diameter of 50 µm

could be produced, as could grooves in the glass; these could then be subsequently filled with metal to form conductive tracks. Metallisation had been achieved using electroless nickel and copper, preceded by deposition of a self-assembling monolayer on the glass, which helped with adhesion of the metal. Adhesion of copper and nickel was good with thin coatings, but at higher thicknesses the adhesion decreased. Various techniques had been developed to bond the layers of the glass together and the lamination quality had been evaluated using a three point bend test and a crack opening test. Using the above developed techniques, single layer glass circuit patterns had been produced and work on multilayer structures was currently underway. David concluded by summarising the work undertaken and acknowledged that the funding for this work was provided by the Innovative Electronics Manufacturing Research Centre (IEMRC).

The third presentation was given by Krzysztof Malecki of Wroclaw University of Technology and it covered a numerical study of heat flow and load distribution during chip to wafer bonding in a vacuum. An advanced chip to wafer hermetic bonding process (AC2W) was described which used a semi-automatic EVG 540C2W bonder. A computer simulation of the wafer level hermetic bonding process was described which showed the temperature field distribution across the assembly and the subsequent deformations. The use of a compliant layer was shown to give an improvement in deformation. It had been concluded that the processes described demanded strong stability and repeatability of the process parameters. Use of low-cost graphite foil as a compliant layer reduced the overall cost of the process, while offering stress reductions and enhanced performance.

The final paper of the session was given by C. P. Wong of Georgia Institute of Technology and was on the incorporation of conjugated molecular wires into anisotropic conductive adhesives. He began by giving an overview of electrically conductive adhesives and, in particular, he focussed on anisotropic materials and their advantages and disadvantages. They were described as being environmentally friendly with mild processing conditions and fine pitch capability. Self assembling monolayers based on thiol chemistry were then introduced along with the mechanisms of conduction in anisotropically conductive adhesives (ACAs). The relationship between work function and tunnel resistivity was shown. The thermal reactions of silver particles such as oxidation were also shown and XPS had been carried out to characterise the surface structure of the oxide particles. Surface oxidation could be removed using an organic acid. Raman Spectroscopy had been used extensively to characterise the nature and molecular alignment of organic materials on the surface of the silver particles. From this work it had been possible to conclude that molecular wires could remove silver oxides and replace contaminants on the surface of the silver particles. This allowed improvements in the electrical

conductivity of these adhesives. Further work was to be undertaken to study the reliability of ACA joints using these molecular wires.

In the second morning session, B5 on 'Materials for Advanced Packaging II' the first presentation was given by Chang-Woo Lee of the Korea Institute of Industrial Technology. This paper was on the dispersion of silicon carbide nano-particles (45 to 55 nm spheres) in tin-bismuth alloy solder micro-bumps. With the continuing miniaturisation of electronics there was a growing need for microbumps and low temperature lead-free solders. Tin-bismuth had good properties and it was the material chosen for the incorporation of silicon carbide. Sn-Bi solder bumps were deposited by electroplating on copper on silicon. The plating solution contained SiC particles (0.5 g/l) which were incorporated in the deposited alloy. Ultrasonics were used to keep the particles dispersed in the plating solution. The melting points of the alloy bumps were 139.5°C both with and without the SiC particles. The microstructure of the bumps had been studied with temperature ageing at up to 400 hours at 100°C and there was no influence on IMC growth. Shear and high speed shear test results showed an increase in shear strength for the bumps containing SiC, compared to the standard alloy. The toughness of the solder bumps also increased for those containing SiC.

The second paper was on the inkjet printing of carbon nanotubes and was given by B. K. Lok of the Singapore Institute of Manufacturing Technology. The techniques used for accurately inkjet printing were described and factors such as jet straightness were found to be important. The carbon nanotubes (CNT) were initially ball milled, followed by a chemical treatment. They were then used in a composite ink also containing conducting polymer (PEDOT). Ink jet printing optimisation work had been carried out to determine the best deposition conditions and deposited films had been characterised using AFM. The variation of electrical conductivity with the concentration of CNT-PEDOT in the ink jet solution had also been studied. Higher temperature deposition (60°C) had been found to give better printing performance and enhanced conductivity.

Tony Winster of Henkel UK then presented the results of work carried out with NXP on the wafer backside coating of electrically conductive die attach adhesives of packaging discrete semiconductor devices. The wafer backside process was described and, in this case, the wafer was backside screen printed with adhesive prior to lamination with wafer mounting tape. Non-conductive die attach adhesives were already commonly used at wafer level and the film adhesives were employed in die stacking applications. Traditionally, many devices had used eutectic die attach approaches but these typically required the use of gold which was expensive. There was thus a strong case for a polymeric die attach adhesive and Henkel had developed a new generation material that retained its modulus to high temperatures. This had been

formulated with silver filler to give electrical conductivity and filler levels of up to 80% by weight had been evaluated. Also, the thermal conductivity was about five times greater than for a conventional epoxy. A range of application methods had also been studied and these included spin coating, spray coating and screen printing. In the end, stencil printing had been selected as the preferred method, as it was already a widely used industrial technique. Devices had been built by NXP using both eutectic and adhesive methods and, although the thermal performance of the devices was better using eutectic, the adhesive bonded devices were well within specification. Accelerated testing had not shown any reliability issues.

Giving his second presentation of the morning David Hutt of Loughborough University then presented 'Adhesion of Thermoplastics to Materials used in Electronics (Tin)'. The background drivers for this work were described and there was said to be a requirement to move away from thermosetting to thermoplastic materials. This allowed techniques such as injection moulding to be used and the materials were more recyclable. A substrateless process was then described in which a carrier film was used during moulding but which was subsequently removed to enable interconnects to be formed. Basic demonstrator circuits were shown and these had highlighted issues with the shrinkage of the polymers and the ability to form good interconnects. Work was underway to understand the wetting and adhesion of the thermoplastics to materials such as tin. This would use techniques such as AFM to place tin particles and to measure the adhesion forces.

The final presentation of the session was by Wolfgang Muller from the Technical University Berlin and was on the use of nanoindentation to determine the mechanical properties of metals used in electronics. The technique had been employed to investigate the metals and intermetallics found in solder joints and the changes that occurred during thermal treatments such as reflow. Sections through solder bumps were shown and their compositions detailed. Nanoindentation could yield properties such as hardness, stiffness, yield stress and elastic modulus from the load versus indentation curves that were generated. Oliver and Pharr had developed the early analytical models that were used in this technique. Data for Vickers hardness, yield stress and Young's modulus was given for tin, which showed anisotropic properties. Young's modulus data for gold, tin and nickel was also shown and compared to the literature values.

Session C5 had a focus on solder joint reliability. C. Q. Cui from Compass Technology Company Ltd in Hong Kong was the first presenter and his paper was on the effect of nickel layer thickness on intermetallic formation and SAC solder joint reliability. As an introduction, the structure of lead-free TBGAs was described and it was stated that a key issue with these packages was missing balls. In this work, tin-silver-copper balls had been used and the substrate was a

740 TBGA with an electrolytic nickel-gold finish having a range of nickel thicknesses from 3.0 to 10.0 microns. The thick nickel was found to out-perform the thin nickel in shear strength testing and it also performed better after high temperature storage. The thin nickel enabled copper to diffuse into the solder, which resulted in the formation of high copper content IMCs after reflow. This layer was found to be the weak link in shear and drop testing. The IMC growth rate was much faster in the samples that had a thin nickel plating and the proposed mechanisms of IMC formation were presented. Samples with the thick nickel (8  $\mu\text{m}$  and 10  $\mu\text{m}$ ) were found to show no incidence of missing balls and they were able to pass packing drop test cycling.

Another of the papers presented in the solder joint reliability session was given by Seong-jae Jeon of Sungkyunkwan University, Korea and it was on the mechanical reliability evaluation of tin-lead solder joints using high speed lap shear testing. The high-speed lap shear test was introduced and it had been used to evaluate samples with 300  $\mu\text{m}$  diameter solder balls and either copper or nickel-gold under-bump metallisation. Stress-strain curves were shown for samples aged at a range of different temperatures from room temperature to 170°C. The shape of these curves was found to vary both with ageing temperature and the strain rate. Three different failure modes were found. For example, at low shear rates ductile failure occurred at all ageing temperatures. Overall, the conclusion from this work was that high speed lap-shear testing could be used to evaluate the drop reliability of solder joints.

One of the final sessions on Thursday was on 'Solder Interconnects' and one of the papers from this session was presented by R. Vemal of Freescale Semiconductor (Malaysia). His paper was on the diffusion of elements in specific lead-free and leaded solder alloys. The lead-free solder was SnAg3.8Cu0.7 and the leaded solder was SnPb36Ag2; they were both on electrolytic nickel-gold on copper. The study methodology and materials used were detailed; the solder joints were baked and thermally aged and then subjected to tensile testing and analysis by SEM and EDX. Data showing diffusion of the elements with ageing was given and, for the leaded solder, copper was the quickest element to react and diffuse into the bulk solder. For the lead-free solder, copper in the SnAgCu helped to form the CuNiSn ternary compound. The gold layer completely dissolved in the bulk solder in the first cycle of the reflow process and subsequent thermal ageing processes to form AuSn. The diffusion of gold into the IMC layers contributed to brittle failures and it was concluded that this was a problem, especially for the SnPb36Ag2 alloy.

Another presentation from this session was given by N. C. Lee of Indium Corporation and in it he asked the question; 'Is it really impossible to combine superior antioxidation and superior print?' With the demand for higher interconnect densities and finer pitch, the

quantities of solder paste deposited were becoming much smaller. In the case of really small solder paste dots and finer solder powders, a problem was that they were more likely to have thicker oxide films on their surfaces. Also, the greater surface area meant that there was actually more of the thicker oxide. This could lead to void formation and thus there could be a need for a higher activity flux. An alternative was to use nitrogen to provide an oxidation barrier. Therefore, new solder pastes were needed that were more resistant to oxidation, that were more efficient oxidation barriers and that had a greater fluxing capacity. They should also have high heat transfer efficiencies. Testing of voiding propensity had been carried out on new formulations using a simulated microvia test with a BGA design that aggravated the voiding potential. Results of these and other tests had confirmed the superior antioxidation and printing performance of the new solder paste formulations.

The third day of the conference continued with the format of six different parallel sessions covering a wide range of subject matter. The first paper in session F5 on 'Solder Joint Reliability II' was given by Tzu Ling Wong of Freescale Semiconductor, Malaysia and was entitled 'FCPBGA with SOP Pad finishing: a study of lead-free solder ball attachment improvement'. With FCPBGA, the industry was said to be moving from ENIG pad finishing to solder on pad and this work was a study of the reliability of such devices with a lead-free solders (SAC387 and Sn3.5Ag). Testing included a cold ball pull test to assess the solder joint strength as formed, after thermal cycling and after six reflow cycles. One of the conclusions from this work was that Sn3.5Ag was the recommended solder ball alloy, as it solved the 'wrinkled ball' issue which was a customer concern and it also gave enhanced solder joint performance.

The next paper was on the superior drop test performance of SAC-Ti alloy solders and was given by N. C. Lee of the Indium Corporation of America. This new alloy had been developed to address some of the issues associated with standard SAC alloys such as fragility. The alloy discussed in this work was SAC0.02Ti (mainly SAC105-0.02Ti), the board finish used for the evaluation was OSP and the devices had an ENIG or NiPdAu finish. Testing and analysis included hardness, microstructure, creep and DSC. The addition of titanium was found to reduce the hardness of the SAC alloy and also there were found to be less (larger) grains than with SAC. The addition of titanium did not have any affect on the melting range of the alloy.

Mrs H. Sosiata of Tokyo University then gave a presentation on a study of spontaneous tin whisker growth that had been carried out using TEM. The driving force for tin whisker growth was compressive stress eg that imparted during tin oxide formation. Specimens were exposed to 85°C/85%RH conditions for up to 2000 hours and the formation of SnO<sub>2</sub> was monitored using high resolution TEM. In these high

humidity conditions, diffusion of oxygen into the tin layer produced the SnO<sub>2</sub>. Additionally, at the higher test temperatures, diffusion of copper into the tin layer produced intermetallic layers of Cu<sub>3</sub>Sn and Cu<sub>6</sub>Sn<sub>5</sub> which also imparted additional stresses.

There then followed another paper on tin whiskering and this one was on the whisker mitigation efficiency of a nickel under layer. This paper was given by Jeffrey ChangBing Lee of Integrated Service Technology in Taiwan. The presentation began with an overview of the factors that may influence tin whisker formation and the current mitigation strategies. In this work the nickel thickness used was between 0.5 and 0.7 microns and the tin thickness was 10 microns. After reflow, the nickel layer had been used up in the formation of IMCs. Experiments were also carried out using a range of tin thicknesses from 2.5 to 10.0 microns. It was concluded that a nickel layer was not good for mitigating tin whisker formation, unless the deposition of a low tin thickness could be well controlled in the plating process.

The final presentation of the session was on the 'fracture toughness assessment of a solder joint using double cantilever beam specimens'. This was given by Shane Loo of Amkor Technology, Singapore. The problem of solder joint reliability in BGA and flip chip joints was outlined and the example of interfacial fractures and failures in joints discussed. Various established methods for testing solder joints were also reviewed before the double cantilever technique was introduced. Reflow conditions were found to have a greater detrimental effect on solder joints as compared to high temperature ageing.

In one of the final sessions of the conference, Kok Soo Goh of Henkel gave a presentation on 'mold compound properties for low warpage array packages'. He began by introducing the key properties of moulding compounds and described how shrinkage had been determined using a moulded bar. Work had been carried out on a wide range of compound formulations to determine their warpage properties. Block warpage versus shrinkage data showed a good correlation with low warpage being associated with low shrinkage materials. Low thermal expansion coefficient ( $\alpha_2$ ) resins also had lower warpage, as did those with higher filler contents (88 to 90%). All the fillers used were spherical. It had additionally been found that increasing the number of die (eg from 1 to 4) in the package also reduced the warpage.

Seung Eun Lee of Samsung Electronics presented a paper on the 'dielectric properties of PCB embedded bismuth niobium films prepared by magnetron sputtering'. High speed devices needed low inductive noise and one solution was to embed passives into the PCB. These needed to be deposited using low temperature (<200°C) processes that were compatible with standard PCB manufacturing routes. The types of materials that could be used to form capacitor structures were then reviewed in terms of their

advantages and disadvantages. Bismuth zinc niobium oxide had been selected because of its low loss, reasonable permittivity (170 to 220) and the fact that it could be deposited by RF sputtering, laser deposition and metal organic deposition. The material had been sputtered onto copper clad laminate materials that had been given a chemical treatment to smooth the surface. The use of different gas mixtures in the sputtering process had an impact on the nature of the deposited films. Actual deposited film dielectric constant values of 100 at 1 MHz with a loss of 15% were reported.

R. Durairaj presented details of work to develop novel online real-time monitoring process for solder paste materials using ultrasonics. The presentation began with a description of the problems to be addressed, the importance of rheology, the nature of solder pastes and their typical printing defects. Solder pastes were non-Newtonian in their behaviour and established techniques were both time consuming and destructive in nature. The new technique could actually be used on jars of solder paste and examples of the ultrasonic data recorded were shown. It was necessary to correlate the actual viscosity of the pastes with the ultrasonic data recorded. Printing trials had been

carried out to correlate the results with the rheological data. Despite this being an initial study, and the fact that more work was required, it had been shown that ultrasonics could indeed be used to monitor batch to batch variations in solder pastes.

The above brief synopses of the presentations are intended to give an overview of the papers that were presented during this extremely well organised and well attended conference. With such a wide range of technical information being presented, the EPTC 10<sup>th</sup> Anniversary Conference really was a special event. The conference organisers are to be thanked for all their hard work and congratulated for making EPTC such a great success. We look forward to 11<sup>th</sup> EPTC 2009, which will take place in one year's time at the same venue.

### Reference

- 1) Proceedings of the EPTC 2008 10<sup>th</sup> Electronics Packaging Technology Conference. Published by IEEE. IEEE Catalogue number: CFP08453-CDR, ISBN: 978-1-4244-2118-3, Library of Congress: 2008900672.



The EPTC 2008 Organising Committee